THAT WHICH IS CLAIMED IS:

1. Method of transmitting data between two devices (D1, MP, D2, PC), by means of a clock wire (CK) and at least one data wire (DT), the clock wire being maintained by default on a logic value A, characterized in that:

- each device can tie the clock wire to an electric potential representing a logic value B that is the opposite of A,
- when a datum is transmitted, the two devices tie the clock wire to B (M12, E11, M21, E21),
- the device to which the datum is sent does not release the clock wire (CK) while it has not read the datum (M23, E14),
- the device sending the datum maintains the datum on the data wire (DT) at least until an instant (t3, t4) when the clock wire (CK) is released by the device to which the datum is sent.

2. Method according to claim 1, in which one of the devices is master and the other slave, the master being distinguished from the slave by the fact that it is the first to tie the clock wire to B (M12, M21) when a datum is transmitted, regardless of the direction in which the datum is transmitted.

3. Method according to claim 2, in which, when the master must send a datum to the slave, the master applies the datum to the data wire (M11), then ties the clock wire to B(M12).

4. Method according to claim 3, in which, when the slave must receive a datum from the master, the slave detects the value B on the clock wire (E10), then ties the clock wire to B(E11) and reads the datum (E12).

5. Method according to claim 4, in which the time (E13) that the slave has to release the clock wire after receiving a datum, is independent of any action by the master, as the master does not send any new datum while the slave has not released the clock wire (M10, M11).

6. Method according to claim 2, in which, when the master must receive a datum from the slave, the master ties the clock wire to B (M21).

7. Method according to claim 6, in which, when the slave must send a datum to the master, the slave detects the value B on the clock wire (E20), then ties the clock wire to B (E21) and applies the datum to the data wire (E22).

8. Method according to claim 7, in which the time (E23) that the slave has to release the clock wire after sending a datum, is independent of any action by the master, as the master does not tie the clock wire to B to request sending a new datum while the slave has not released the clock wire (M10).

9. Method according to one of claims 2 to 8, in which, when the clock wire has the logic value A,

the time that the master has to tie the clock wire to B is independent (M16, M24) of any action by the slave.

10. Method according to one of claims 2 to 9, characterized in that it comprises a step of equipping the slave with a communication interface circuit (HWC) comprising:

- trigger means to automatically tie the clock wire to B when the clock wire changes from A to B,
- an input to apply a clock wire release signal to the trigger means, and
- an output to deliver an information signal (STATUS) that has a first value when the clock wire is tied to B by the trigger means and a second value when the clock wire is released by the trigger means.

11. Method according to claim 10, comprising a step of further providing, in the communication interface circuit:

- means for storing at least one datum, and
- means for automatically applying the datum to the data wire when the clock wire changes from A to B.

12. Method according to one of claims 1 to 11, in which A=1 and B=0.

13. Master-type data transmitting/receiving device (MSTR) comprising a connection terminal to a clock wire (CK), at least one connection terminal to a data wire (DT), and means for tying the clock wire (CK) to an electric potential B representing a logic value that is the opposite of a logic value A, characterized

in that it comprises means for performing the following operations, when a datum (B) is to be sent:

- checking or waiting for the clock wire to have the logic value A (M10),
- applying the datum to the data wire (M11),
- tying the clock wire (M12) to B, then
- releasing the clock wire (M13), and
- maintaining the datum on the data wire at least until an instant (t3, t4) when the clock wire has the logic value A (M14, M10)

14. Device according to claim 13, further comprising means for performing the following operations, when a datum is to be received:

- checking or waiting for the clock wire to have the logic value A (M20),
- tying the clock wire (M21) to B,
- reading the datum on the data wire (M22), then
- releasing the clock wire (M23).

15. Slave-type data transmitting/receiving device (SLV, SLV+HWC) intended to communicate with a master-type device (MSTR) according to one of claims 13 and 14, comprising a connection terminal (CKP) to a clock wire (CK), at least one connection terminal (CDT) to a data wire (DT), and means for tying the clock wire to an electric potential B representing a logic value that is the opposite of a logic value A, characterized in that it comprises means for performing the following operations, when a datum (B) is to be received:

- detecting a change from A to B on the clock wire (E10),
- tying the clock wire (E11) to B,

- reading the datum on the data wire (E12), and
- releasing the clock wire (E14).

16. Device according to claim 15, further comprising means for performing the following operations, when a datum is to be sent:
- detecting a change from A to B on the clock wire (E20),
- tying the clock wire (E21) to B,
- applying the datum to the data wire (E22), and
- releasing the clock wire (E24).

17. Synchronous data transmission system, characterized in that it comprises a master-type device (MSTR) according to one of claims 13 and 14 linked by a clock wire (CK) and at least one data wire (DT) to a slave-type device (SLV) according to one of claims 15 and 16.

18. Slave-type communication interface circuit (HWC) linked or intended to be linked by means of a clock wire (CK) and at least one data wire (DT) to a master-type device (MSTR) according to one of claims 13 and 14, characterized in that it comprises:
- means for tying the clock wire to an electric potential B representing a logic value that is the opposite of a logic value A,
- trigger means (FD1, FD2) to automatically tie the clock wire to B when the clock wire changes from A to B,
- an input (ACK) to apply a clock wire release signal to the trigger means, and

- an output to deliver an information signal (STATUS) that has a first value when the clock wire is tied to B by the trigger means and a second value when the clock wire is released by the trigger means.

19. Communication interface circuit according to claim 18, further comprising:

- means (FD4) for storing at least one datum, and
- means (FD3, FD4) for automatically applying the datum to the data wire when the clock wire changes from A to B.